Chapter 7

Tracking of Spread Spectrum Signals

7.1 Introduction

As discussed in the last chapter, there are two parts to the synchronization process. The first stage is often termed acquisition and typically obtains initial, coarse timing synchronization. The second is termed tracking and involves fine tuning the delay estimate. Tracking occurs throughout the duration of the communication. This procedure is presented in Figure 7.1.

In this chapter we will investigate code tracking. Code tracking is analogous to phase tracking in conventional digital communication systems. Much of the analysis can be directly borrowed from phase tracking analysis. There are several well-known techniques for performing tracking including the Delay Lock Loop (DLL), the Tau-Dither Loop, and the Double-Dither Loop. In this chapter we will focus on the Delay Lock Loop.

7.2 The Delay Lock Loop

Perhaps the most common form of tracking is the delay lock loop or what is often termed the Early-Late Gate. The coherent Early-Late Gate is plotted in Figure 7.2. The basic idea behind the circuit is that if we attempt to despread the signal with a version of the spreading code that is either early or late, we obtain less then full energy. The difference between these two despreader outputs (on average) tells us whether the current timing is ahead or behind the true delay. To understand this consider Figure 7.2.

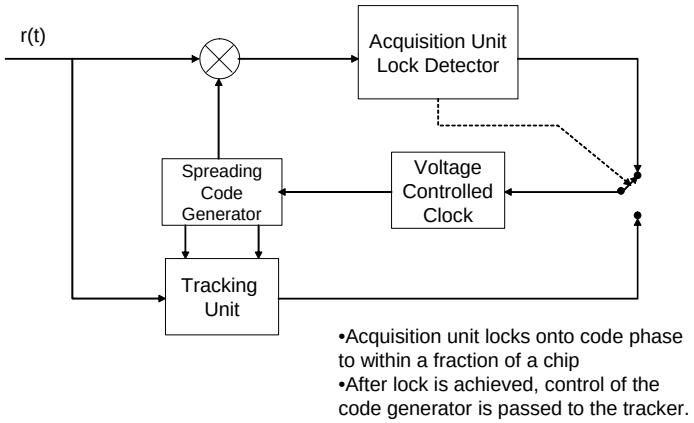


Figure 7.1: Block Diagram of Synchronization

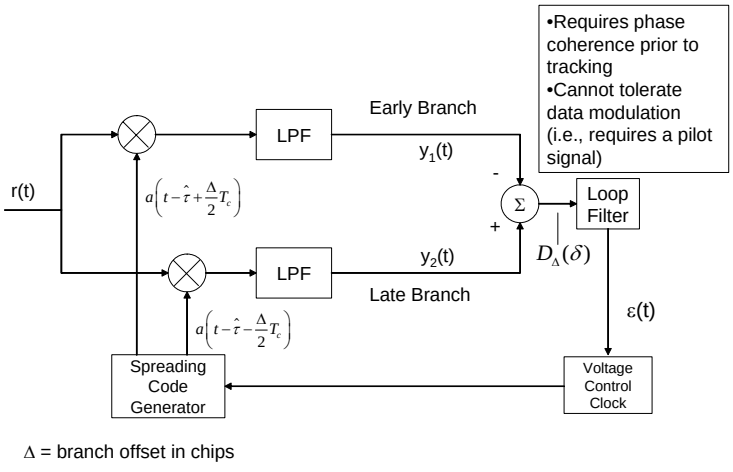


Figure 7.2: Block Diagram of a Coherent Delay Lock Loop

As can be seen from the figure, the output of the early branch is

$$\begin{aligned} y_+(t) &= \int_t^{t+T} \sqrt{P}a\left(\lambda - \hat{\tau} + \frac{\Delta}{2}T_c\right) a(\lambda - \tau)d\lambda \\ &= R_a\left(\tau - \hat{\tau} + \frac{\Delta}{2}T_c\right) \\ &= R_a\left(\left[\delta + \frac{\Delta}{2}\right]T_c\right) \end{aligned} \tag{7.1}$$

while the output from the late branch is

$$\begin{aligned} y_-(t) &= \int_t^{t+T} \sqrt{P}a\left(\lambda - \hat{\tau} - \frac{\Delta}{2}T_c\right) a(\lambda - \tau)d\lambda \\ &= R_a\left(\tau - \hat{\tau} - \frac{\Delta}{2}T_c\right) \\ &= R_a\left(\left[\delta - \frac{\Delta}{2}\right]T_c\right) \end{aligned} \tag{7.2}$$

Thus, the input to the loop filter is

$$D_\Delta(\delta) = R_a\left(\left[\delta - \frac{\Delta}{2}\right]T_c\right) - R_a\left(\left[\delta + \frac{\Delta}{2}\right]T_c\right) \tag{7.3}$$

This is plotted in Figure 7.4 for an arbitrary value of Δ. Note that while the discriminator characteristic is non-linear in general, it is linear in the region near $\delta = 0$. Thus, provided that the difference between the estimated delay and the true delay is no more than a fraction of a chip, the discriminator will operate in its linear range. The size of the linear range, as well as the slope depends on the value of Δ. This can be seen in Figure 7.5 where the S-curve is plotted for $\Delta = \frac{1}{2}$, $\Delta = 1$, $\Delta = \frac{3}{2}$, and $\Delta = 2$. When $\Delta = \frac{1}{2}$, the linear range is $-0.25T_c \leq t \leq 0.25T_c$. Further, the slope is $2\left(1 + \frac{1}{N}\right)$. By increasing Δ to a full chip, the slope remains unchanged, but the linear region is increased to $-0.5T_c \leq t \leq 0.5T_c$. However, increasing Δ further reduces the linear range back to $-0.25T_c \leq t \leq 0.25T_c$ again. However, notice that the characteristic is also linear for $-0.75T_c \leq t \leq -0.25T_c$ and $0.25T_c \leq t \leq 0.75T_c$ although with a lower slope of $\left(1 + \frac{1}{N}\right)$. By increasing Δ to 2, the first linear region is reduced to zero, while the second linear region is increased to $-T_c \leq t \leq T_c$

7.2.1 Impact of Pulse Shape

In the previous section we analyzed the tracking discriminator characteristic assuming a square pulse shape. However, due to the large bandwidth requirements of square pulses they are rarely used in wireless applications. Thus, we need to evaluate the impact of other pulse shapes. As as an example consider the optimal pulse shape in terms of bandwidth, the sinc pulse. The sinc pulse can be written as

$$p\left(t\right) = T_c \sin c\left(\frac{t}{T_c}\right) \tag{7.4}$$

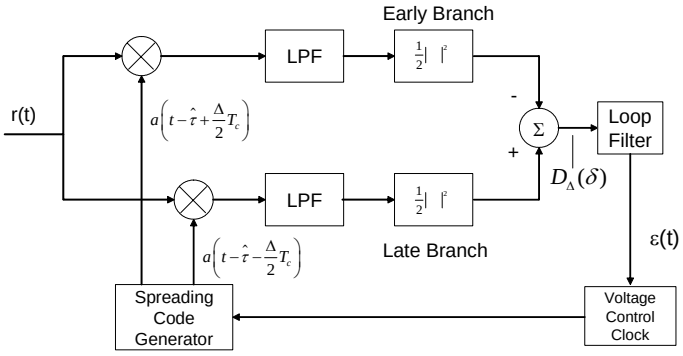


Figure 7.3: Block Diagram of the Early-Late Gate Tracking Loop

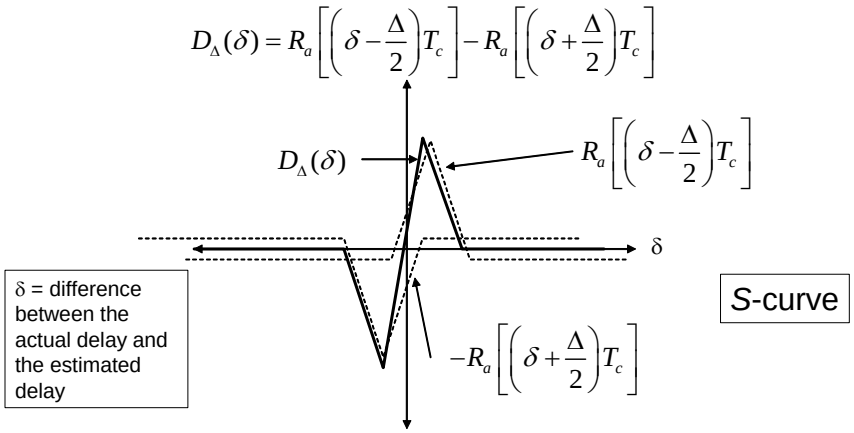


Figure 7.4: Coherent DLL S-Curve

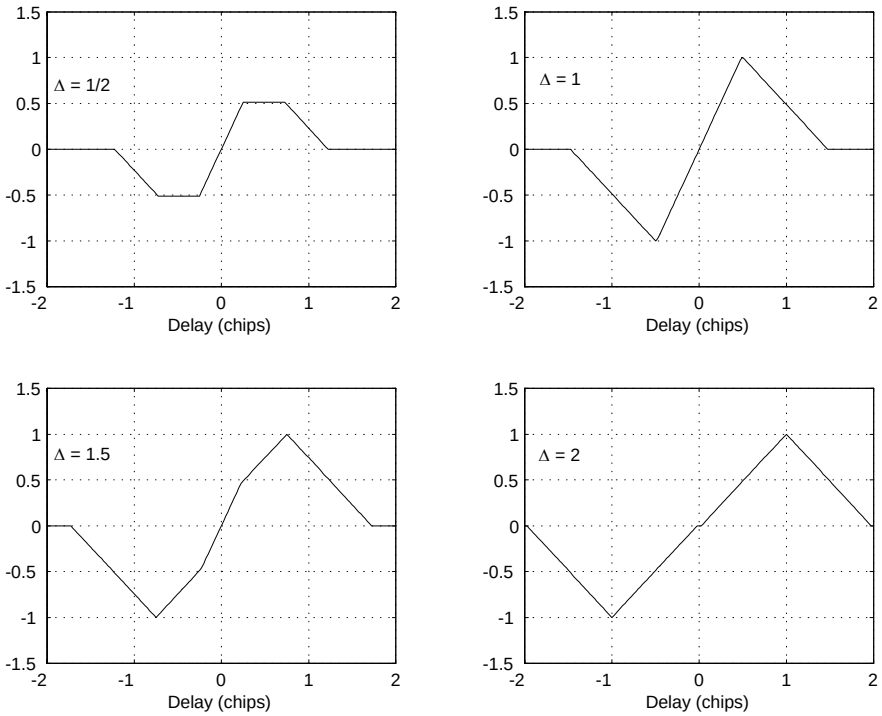


Figure 7.5: Coherent DLL Discriminator S-curve Characteristic for $\Delta = 1/2, 1, 1.5, 2$

As discussed in Chapter 5, the autocorrelation of the spreading waveform is dominated by the pulse autocorrelation function. We can find the autocorrelation function of the sinc pulse as

$$\begin{aligned} R_p(\tau) &= p(t) * p(-t) && (7.5)\\ &= p(t) * p(t) && (7.6) \end{aligned}$$

where the second line results from the fact that the sinc pulse is symmetric. Using the Fourier Transform, we can write

$$R_p(\tau) = F^{-1}\{P(f)\,P(f)\} \tag{7.7}$$

where $P(f)$ is the Fourier Transform of the pulse shape. Thus, we can write

$$\begin{aligned} R_p(\tau) &= F^{-1}\{rec(fT_c)\,rec(fT_c)\} && (7.8)\\ &= F^{-1}\{rec(fT_c)\} && (7.9)\\ &= T_c \sin c\left(\frac{t}{T_c}\right) && (7.10) \end{aligned}$$

Thus, the autocorrelation function is the same as the pulse shape. Assuming the ideal sequence autocorrelation $C_{\mathbf{aa}}(n) = \begin{cases} 1 & n = 0 \\ 0 & n \neq 0 \end{cases}$, the discriminator characteristic can be written as

$$\begin{aligned} D_\Delta(\delta) &= R_p\left(\left[\delta - \frac{\Delta}{2}\right] T_c\right) - R_p\left(\left[\delta + \frac{\Delta}{2}\right] T_c\right) && (7.11)\\ &= \sin c\left(\left[\delta - \frac{\Delta}{2}\right]\right) - \sin c\left(\left[\delta + \frac{\Delta}{2}\right]\right) && (7.12) \end{aligned}$$

The resulting characteristic is plotted in Figure 7.6. We can see that like the square pulse, there exists a nearly linear region with a slope of approximately 2 over the range $\left(-\frac{1}{2}, \frac{1}{2}\right)$. Like in the case of a square pulse, the discriminator will work properly provided that the error stays within this linear region.

Further, consider two additional pulses that are commonly used the raised cosine pulse (roll-off factor of 0.25) and the pulse used in the IS-95 standard [1]. The pulses are plotted along with a square pulse in Figure 7.7. Using the same development as shown above for the sinc pulse, we can derive the autocorrelation fuction and the resulting discriminator characteristic for each of the pulse shapes. The discriminator characteristic for each pulse is given in Figure 7.8 for $\Delta = 1$, $\Delta = 1/2$, and $\Delta = 3/2$ respectively. We can see that the other pulse shapes provide similar trends as the square pulse. Setting $\Delta = 1$ provides the best characteristic as $\Delta = 1/2$ impacts the size and slope of the linear region while $\Delta = 1.5$ slightly distorts the linear region.

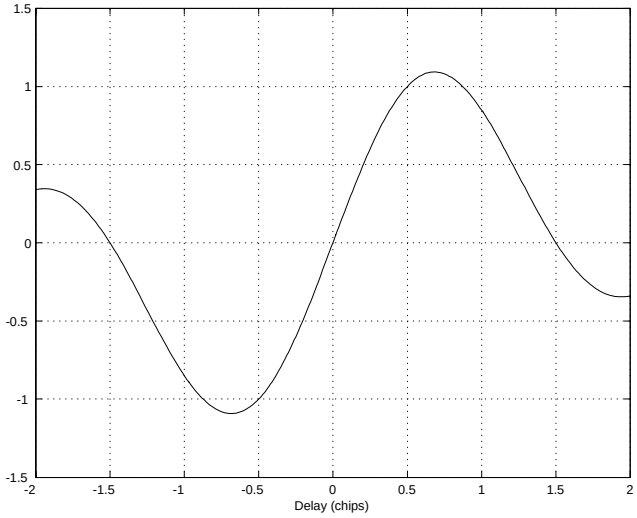


Figure 7.6: Discriminator Characteristic for Sinc Pulse when $\Delta = 1$.

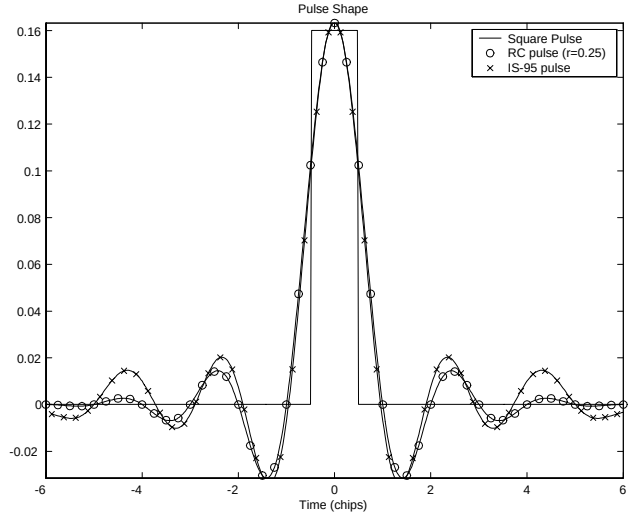


Figure 7.7: Commonly Considered Pulse Shapes

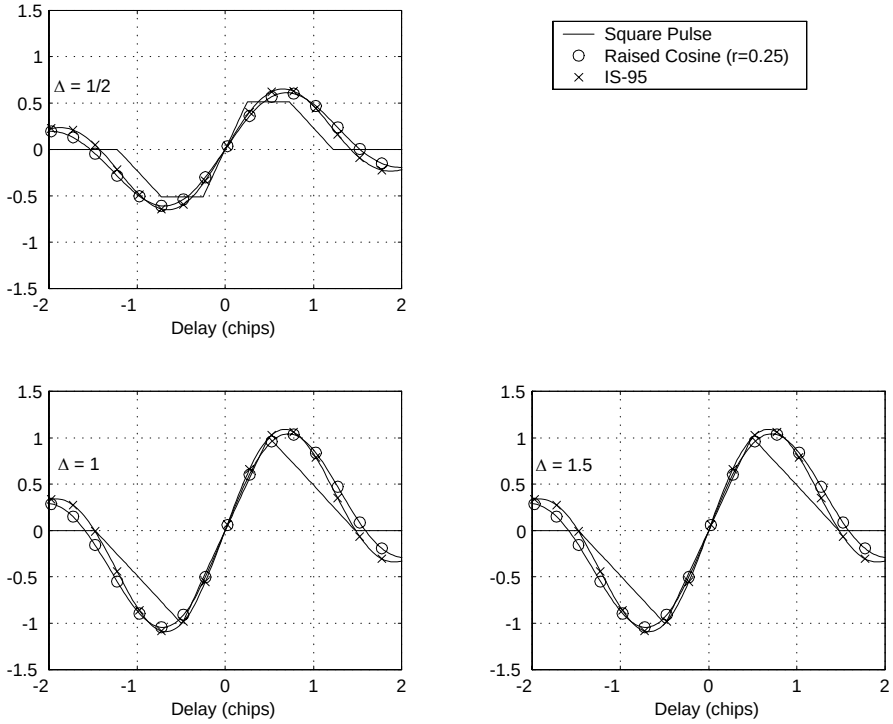


Figure 7.8: Comparison of Coherent Discriminator DLL S-curve Characteristics for Various Pulse Shapes and Delay

7.3 The Non-coherent Delay Lock Loop

A main limitation of the coherent delay lock loop is that it cannot tolerate data modulation. Thus, it requires a pilot signal for proper operation. In many cases pilot signals cannot be afforded since they result in wasted power. A solution to this problem is the non-coherent delay lock loop shown in Figure **??**. In this loop, the output of the despreading operation on both the early and the late branch are squared prior to subtracting the early result from the late result. While this changes the discriminator characteristic, it still results in a linear region around $\delta = 0$ and thus allows for proper operation. Specifically the discriminator characteristic is [2]

$$D_\Delta(\delta) = R_a^2\left(\left[\delta - \frac{\Delta}{2}\right]T_c\right) - R_a^2\left(\left[\delta + \frac{\Delta}{2}\right]T_c\right) \tag{7.13}$$

For $\Delta \geq 1$, this results in

$$\Delta_a(\delta) = \begin{cases} 0 & -N+1+\frac{\Delta}{2} < \delta \leq -\left(1+\frac{\Delta}{2}\right) \\ \frac{1}{N^2} - \left[1+\left(1+\frac{1}{N}\right)\left(\delta+\frac{\Delta}{2}\right)\right]^2 & -\left(1+\frac{\Delta}{2}\right) < \delta \leq -\frac{\Delta}{2} \\ \frac{1}{N^2} - \left[1-\left(1+\frac{1}{N}\right)\left(\delta+\frac{\Delta}{2}\right)\right]^2 & -\frac{\Delta}{2} < \delta \leq -\left(1-\frac{\Delta}{2}\right) \\ 2\left(1+\frac{1}{N}\right)\left[2-\left(1+\frac{1}{N}\right)\Delta\right]\delta & -\left(1-\frac{\Delta}{2}\right) < \delta \leq \left(1-\frac{\Delta}{2}\right) \\ \left[1+\left(1+\frac{1}{N}\right)\left(\delta-\frac{\Delta}{2}\right)\right]^2 - \frac{1}{N^2} & \left(1-\frac{\Delta}{2}\right) < \delta \leq \frac{\Delta}{2} \\ \left[1-\left(1+\frac{1}{N}\right)\left(\delta-\frac{\Delta}{2}\right)\right]^2 - \frac{1}{N^2} & \frac{\Delta}{2} < \delta \leq \left(1+\frac{\Delta}{2}\right) \end{cases} \tag{7.14}$$

For $\Delta \leq 1$ the discriminator characteristic is

$$\Delta_a(\delta) = \begin{cases} 0 & -N+1+\frac{\Delta}{2} < \delta \leq -\left(1+\frac{\Delta}{2}\right) \\ \frac{1}{N^2} - \left[1+\left(1+\frac{1}{N}\right)\left(\delta+\frac{\Delta}{2}\right)\right]^2 & -\left(1+\frac{\Delta}{2}\right) < \delta \leq -\left(1-\frac{\Delta}{2}\right) \\ -2\left(1+\frac{1}{N}\right)\Delta\left[1+\left(1+\frac{1}{N}\right)\delta\right] & -\left(1-\frac{\Delta}{2}\right) < \delta \leq -\frac{\Delta}{2} \\ 2\left(1+\frac{1}{N}\right)\left[2-\left(1+\frac{1}{N}\right)\Delta\right]\delta & -\frac{\Delta}{2} < \delta \leq \frac{\Delta}{2} \\ 2\left(1+\frac{1}{N}\right)\Delta\left[1+\left(1+\frac{1}{N}\right)\delta\right] & \frac{\Delta}{2} < \delta \leq 1-\frac{\Delta}{2} \\ \left[1+\left(1+\frac{1}{N}\right)\left(\delta+\frac{\Delta}{2}\right)\right]^2 - \frac{1}{N^2} & \frac{1}{-}\Delta 2 < \delta \leq \left(1+\frac{\Delta}{2}\right) \end{cases} \tag{7.15}$$

As can be seen, the region around $\delta = 0$ is linear. The size of the linear region depends on the value of Δ. For $\Delta > 1$, the linear region is $-\left(1-\frac{\Delta}{2}\right) < \delta \leq \left(1-\frac{\Delta}{2}\right)$ whereas when $\Delta \leq 1$, the region is $-\frac{\Delta}{2} < \delta \leq \frac{\Delta}{2}$. In either case, we see that the linear region is maximized when $\Delta = 1$. Examples of the Non-coherent DLL discriminator characteristic are plotted in Figure 7.9

7.4 Loop Analysis

In order to analyze the performance of the delay lock loop we must create a model for the delay and the resulting tracking error. A straightforward non-linear model of the loop is presented in Figure 7.10. The time varying delay of the signal normalized by the chip period comes into the loop and is the compared

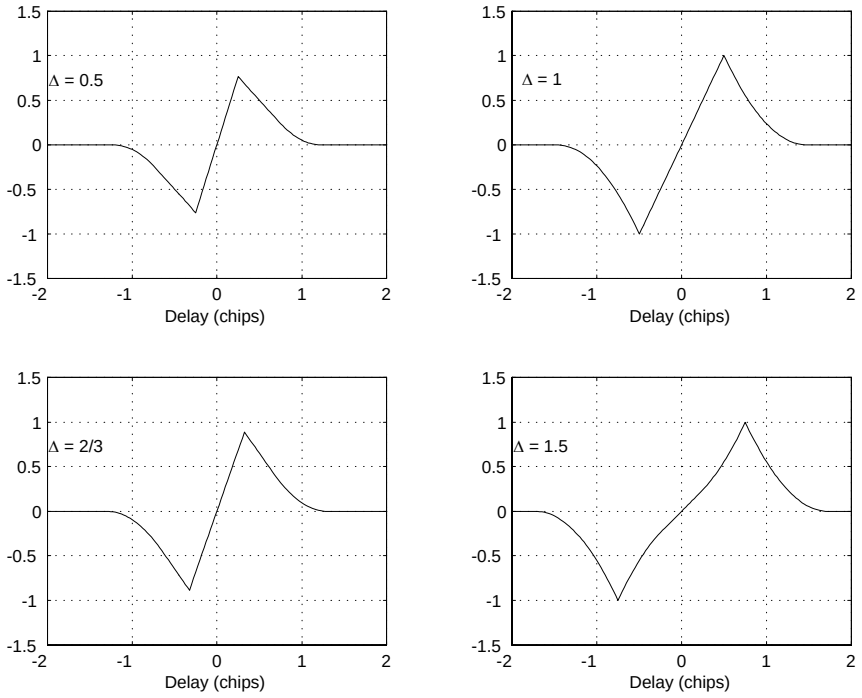


Figure 7.9: Non-coherent DLL Discriminator S-curve Characteristic for $\Delta = 1/2, 1, 2/3, 1.5$

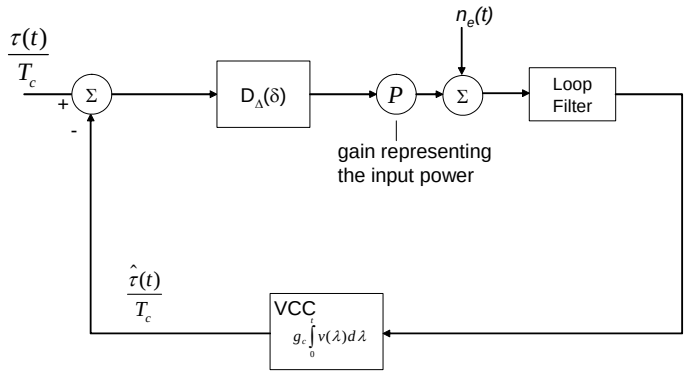


Figure 7.10: Non-linear Model of the Delay Lock Loop

to the current delay estimate. The difference is input into the discriminator. The output of the discriminator is determined by the non-linear discriminator characteristic. The signal-to-noise ratio of the input signal is captured by a gain $\sqrt{P}$ multiplying the discriminator output before tracking noise is added. The noisy signal is filtered before driving a voltage controlled clock which can be represented by a simple integrator. The output of the integrator is delay estimate which is compared to the input delay.

The non-linear model of the loop is not particularly convenient to analyze. If the delay estimate is within a fraction of a chip of the true estimate (this will depend on the accuracy of the acquisition circuitry and the tracking loop performance), the discriminator will operate within its linear range. Provided that this is the case, the loop can be modeled using a linear version of the loop. This is given in Figure 7.11. The discriminator is replaced by a linear gain term $K_d = P\left[\frac{dD(\delta)}{d\delta}\right]_{\delta=0}$. Since the model is linear, the noise can be moved to the input of the loop, after scaling by the discriminator gain. Evaluating the discriminator gain:

$$K_d = 4P\left(1+\frac{1}{N}\right)\left[1-\left(1+\frac{1}{N}\right)\frac{\Delta}{2}\right] \tag{7.16}$$

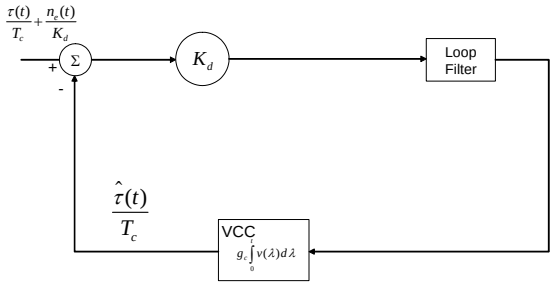


Figure 7.11: Linear Model of the Delay Lock Loop

7.4.1 Discrete Analysis

The loop can be analyzed using standard discrete time analysis (i.e., z-transform) techniques. Let us define the loop filter as $\alpha F(z)$ and the model the integrator (accumulator) as $\frac{z^{-1}}{1-z^{-1}}$ where z^{-1} is the standard delay operator in the z-transform domain. The output of the accumulator can then be found as

$$\begin{aligned}
\frac{\hat{\tau}(z)}{T_c} &= \left(\frac{\tau(z)}{T_c} - \frac{\hat{\tau}(z)}{T_c}\right) \frac{\alpha K_d F(z) z^{-1}}{1 - z^{-1}} \\
&= \frac{\tau(z)}{T_c} \frac{\frac{\alpha K_d F(z) z^{-1}}{1-z^{-1}}}{1 + \frac{\alpha K_d F(z) z^{-1}}{1-z^{-1}}} \\
&= \frac{\tau(z)}{T_c} \frac{H(z)}{1 + H(z)}
\end{aligned} \tag{7.17}$$

Now, letting $F(z) = 1$,

$$\begin{aligned}
\frac{\hat{\tau}(z)}{T_c} &= \frac{\tau(z)}{T_c} \frac{\frac{\alpha K_d z^{-1}}{1-z^{-1}}}{1 + \frac{\alpha F(z) z^{-1}}{1-z^{-1}}} \\
&= \frac{\tau(z)}{T_c} \frac{\alpha K_d z^{-1}}{1 - z^{-1}(1 - \alpha K_d)}
\end{aligned} \tag{7.18}$$

Now, for $\Delta = T_c$, $K_d \approx 2P$. Thus,

$$\frac{\hat{\tau}(z)}{T_c} = \frac{\tau(z)}{T_c} \frac{2\alpha P z^{-1}}{1 - z^{-1}(1 - 2\alpha P)} \tag{7.19}$$

Thus, for an arbitrary input $\tau(z)$ we can determine a loop response $\hat{\tau}(z)$. Additionally, we can compute the loop error response as

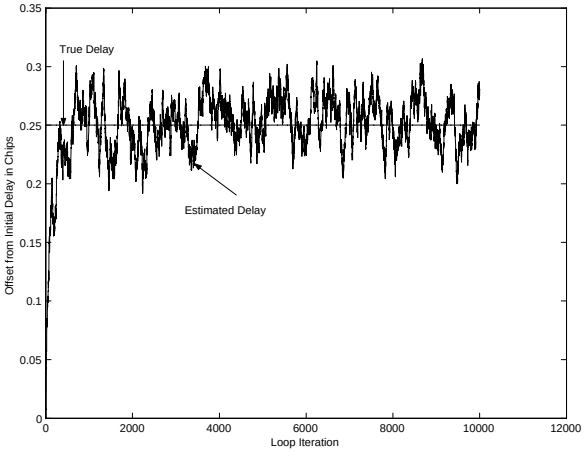
$$\begin{aligned} \tau_e(z) &= \left(\frac{\tau(z)}{T_c} - \frac{\hat{\tau}(z)}{T_c}\right) \\ &= \frac{\tau(z)}{T_c}\frac{1-z^{-1}}{1-z^{-1}(1-2\alpha P)} \end{aligned} \tag{7.20}$$

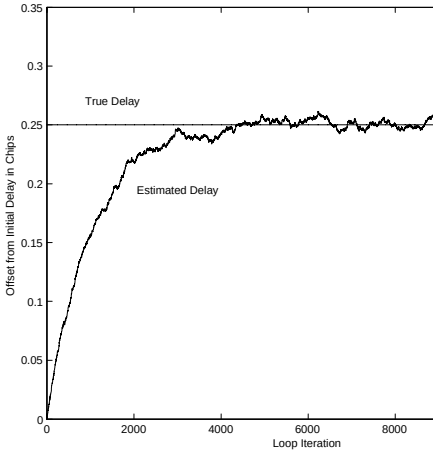
The main control parameter in this case is the filter gain α. We can decrease the loop response to noise by decreasing α. However, this also has the effect of increasing the loop response time. As an example, consider a step input $\frac{\Delta\tau}{T_c}$

$$\begin{aligned} \tau_e(z) &= \frac{\Delta\tau}{T_c}\frac{1}{1-z^{-1}}\frac{1-z^{-1}}{1-z^{-1}(1-2\alpha P)} \\ &= \frac{\Delta\tau}{T_c}\frac{1}{1-z^{-1}(1-2\alpha P)} \end{aligned} \tag{7.21}$$

As an example consider a step input change of $0.25T_c$. Figure **??** plots a sample loop response for an input SNR of 10dB, $F(z) = 1$ and $\alpha = 0.01$. It can be seen that the loop responds very quickly, converging in a few hundred samples. However, there is significant jitter in the response as the delay estimate varies between $0.2T_c$ and $0.3T_c$. If we decrease α by a factor of 10, the loop responds much more slowly, but the jitter is reduced considerably as shown in Figure **??**.

Finally, consider a constantly changing input delay. Specifically in Figure 7.12 the response of the loop to an input with a slew rate of $0.0001T_c$ per sample is plotted. The initial delay value is $0.25T_c$ and $\alpha = 0.01$. The loop is able to track the change, although the estimate is somewhat noisy.





Loop Response to Step Input ($\Delta\tau = 0.25T_c$, SNR = 10dB, $\alpha = 0.01$)Loop Response to Step Input ($\Delta\tau = 0.25T_c$, SN

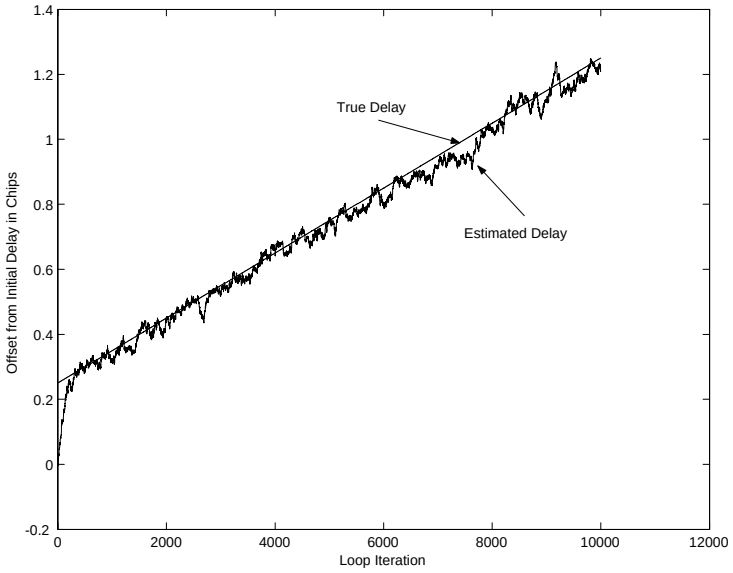


Figure 7.12: Loop Response to Ramp Input ($\Delta\tau = 0.25T_c$, slew rate $0.0001T_c$ /sample, SNR = 10dB, $\alpha = 0.01$)

7.4.2 Non-coherent DLL Performance

The non-coherent DLL can be analyzed using a linear loop model in the same manner as the coherent loop. The only adjustment that must be made is the discriminator gain which is slightly different for the non-coherent loop. We would like to analyze the loop jitter, that is the variance in the delay estimate. This can be found as

$$\sigma_\delta^2 = \int_{-\infty}^{\infty} S_n(f) \left|H(f)\right|^2 df \tag{7.22}$$

where $S_n(f)$ is the input noise power spectral density and $H(f)$ is the loop transfer function. It can be shown that the noise at the output of the discriminator is white with two-sided density

$$\frac{\eta}{2} = 2N_o^2 B_N + N_o P \left\{ R_a^2 \left[\left(\delta - \frac{\Delta}{2} \right) T_c \right] + R_a^2 \left[\left(\delta + \frac{\Delta}{2} \right) T_c \right] \right\} \tag{7.23}$$

Now the jitter is then $\sigma_\delta^2 = \frac{\eta}{2}\frac{1}{K_d^2}W_L$ where W_L is the two-sided loop bandwidth. Assuming that $\Delta = T_c$, $N >> 1$, and δ 0,

$$\begin{aligned}
\frac{\eta}{2} &= 2N_o^2 B_N + N_o P\left\{R_a^2\left[\left(\delta - \frac{\Delta}{2}\right)T_c\right] + R_a^2\left[\left(\delta + \frac{\Delta}{2}\right)T_c\right]\right\} \\
&= 2N_o^2 B_N + N_o P\left\{R_a^2\left[\left(-\frac{\Delta}{2}\right)T_c\right] + R_a^2\left[\left(+\frac{\Delta}{2}\right)T_c\right]\right\} \\
&= 2N_o^2 B_N + N_o P\left\{2\left(1 - \frac{\Delta}{2}\right)^2\right\} \\
&= 2N_o^2 B_N + \frac{1}{2}N_o P \qquad (7.24)
\end{aligned}$$

Returning to the equation for loop jitter

$$\sigma_\delta^2 = \left(2N_o^2 B_N + \frac{1}{2}N_o P\right)\frac{1}{K_d^2}W_L \qquad (7.25)$$

The gain of the discriminator characteristic can be found to be

$$K_d = 2P\left[1 - \frac{\Delta}{2}\right] \qquad (7.26)$$

Thus, letting $\Delta = 1$

$$\begin{aligned}
\sigma_\delta^2 &= \left(2N_o^2 B_N + \frac{1}{2}N_o P\right)\frac{1}{\left(2P\left[1 - \frac{\Delta}{2}\right]\right)^2}W_L \\
&= \left(2N_o^2 B_N + \frac{1}{2}N_o P\right)\frac{1}{P^2}W_L \\
&= \left(\frac{4N_o B_N}{P} + 1\right)\frac{N_o}{2P}W_L \\
&= \left(\frac{4}{\rho_{IF}} + 1\right)\frac{1}{\rho_L} \qquad (7.27)
\end{aligned}$$

where ρ_L is the loop SNR and ρ_{IF} is the SNR at the IF bandpass filter. In general (any value of Δ) the jitter is

$$\sigma_\delta^2 = \left(\frac{1}{\rho_{IF}\left(1 - \frac{\Delta}{2}\right)^2} + 1\right)\frac{1}{\rho_L} \qquad (7.28)$$

As an example, consider the plots of jitter versus loop SNR (ρ_L) in Figure 7.13. The bandwidth at IF is 100 times the loop bandwidth. We can see that Δ makes little difference. However, recall that Δ can have a large impact on the linear range of discriminator. Figure 7.14 plots jitter versus loop SNR for the case where the IF bandwidth is 1000 times the loop bandwidth. For the larger IF bandwidth, there is more noise at the input which increases tracking jitter for a constant loop SNR. Again, we see that Δ has little impact.

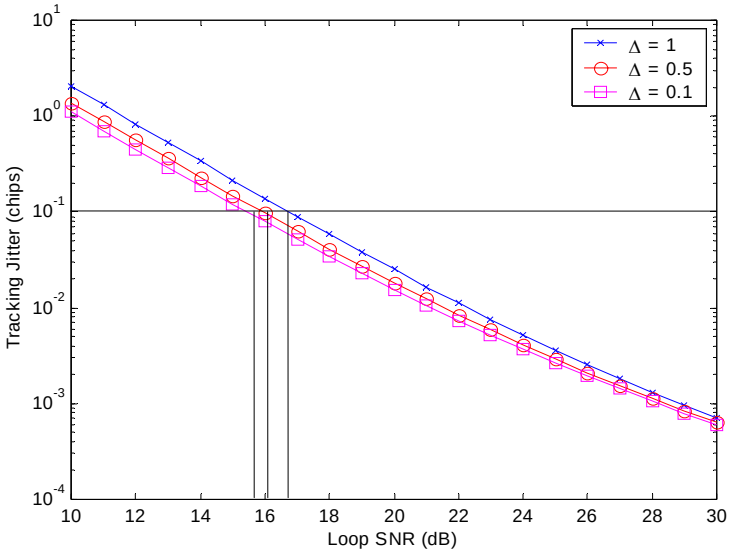


Figure 7.13: Example of Timing Jitter ($B_{IF} = 100B_L$, SNR = 10dB, $\alpha = 0.01$)

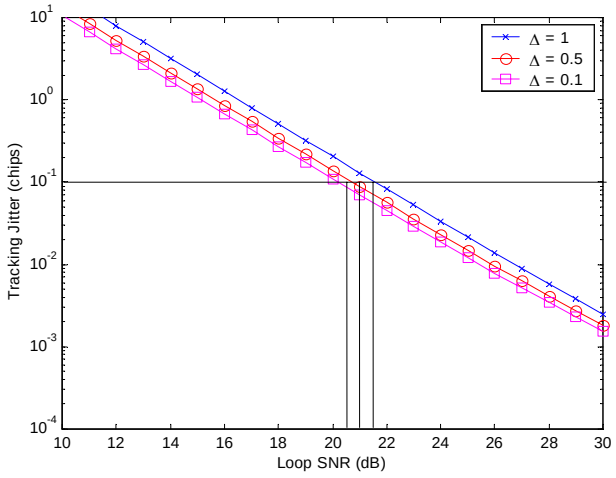


Figure 7.14: Example of Timing Jitter ($B_{IF} = 1000B_L$, SNR = 10dB, $\alpha = 0.01$)

7.5 Laplace Analysis

Another technique for investigating the performance of a tracking loop is to investigate it in the analog domain via the Laplace transform. The linear model for the delay lock loop in the Laplace domain is presented in Figure 7.15. The model is similar to the discrete domain version with the exception that the integrator is now represented by $\frac{1}{s}$ and all transforms are in the Laplace domain.

The transfer function of the loop $H(s) = frac\hat{\tau}(s)\tau(s)$ can be found from the linear model. Specifically,

$$\begin{aligned} \frac{\hat{\tau}(s)}{T_c} &= K_d F(s) \frac{g_c}{s} \left\{ \frac{\tau(s)}{T_c} - \frac{\hat{\tau}}{(} s) T_c \right\} \\ \frac{\hat{\tau}(s)}{T_c} &= \left\{ 1 + K_d F(s) \frac{g_c}{s} \frac{\tau(s)}{T_c} \right\} \end{aligned} \tag{7.29}$$

Solving for $H(s)$ results in

$$H(s) = \frac{K_d F(s) g_c}{1 + K_d F(s) g_c} \tag{7.30}$$

We can also easily find the tracking error with respect to the input signal as

$$\begin{aligned} E(s) &= \frac{\tau(s)}{T_c} - \frac{\hat{\tau}(s)}{T_c} \\ &= \frac{\tau(s)}{T_c} \left[1 - H(s) \right] \\ &= \frac{\tau(s)}{T_c} \frac{s}{s + K_d g_c F(s)} \end{aligned} \tag{7.31}$$

We are interested in two aspects of the error signal: the steady state error and the response time. We would like to examine the impact that $F(s)$ has on these two items. We shall first examine the steady state error. The steady state error can be found as $\lim_{s \leftarrow 0} sE(s)$. Let us first consider a step change to the delay: $\tau(t) = Au(t)$. The steady state error e can be found as

$$\begin{aligned} e &= \lim_{s \leftarrow 0} sE(s) \\ &= \lim_{s \leftarrow 0} s \frac{\tau(s)}{T_c} \frac{s}{s + K_d g_c F(s)} \\ &= \lim_{s \leftarrow 0} s \frac{A}{s} \frac{s}{s + K_d g_c F(s)} \\ &= \lim_{s \leftarrow 0} \frac{As}{s + K_d g_c F(s)} \\ &= 0 \end{aligned} \tag{7.32}$$

Thus, for a step input the loop will eventually track the change regardless of the loop filter forcing the steady state error to zero.

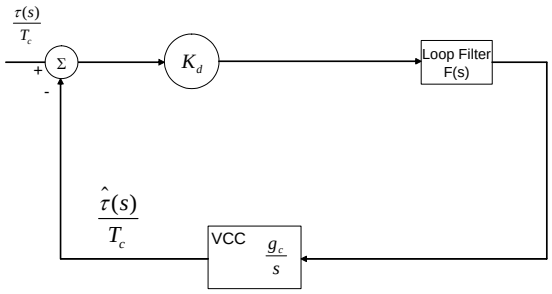


Figure 7.15: A Linear Model of the Coherent Delay Lock Loop in the Laplace Transform Domain

To find the error response, let us first examine the all pass filter $F(s) = 1$. The error is then

$$\begin{aligned} E(s) &= \frac{\tau(s)}{T_c} \frac{s}{s + K_d g_c F(s)} \\ &= \frac{A}{s} \frac{s}{s + K_d g_c F(s)} \\ &= \frac{A}{s + K_d g_c F(s)} \end{aligned} \tag{7.33}$$

Taking the inverse Laplace transform

$$e(t) = Ae^{-K_d g_c t} \tag{7.34}$$

Thus, we can see again that the error will eventually decay to zero. The rate of decay depends on the discriminator gain and the integrator constant. An example is plotted in Figure 7.16 for an all pass filter and a step input of $0.25T_c$. In the example, $\Delta = 1$ and $SNR = 10$.

As a second case let us examine a low pass filter as the loop filter. That is

$$F(s) = \frac{\alpha}{s + \alpha} \tag{7.35}$$

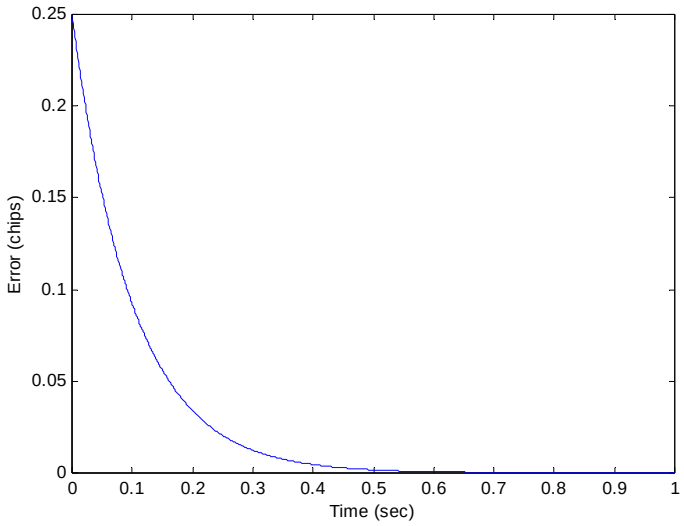


Figure 7.16: Example Error Signal $0.25\mathrm{T}_c$ Step Input

The error signal is then found in the Laplace domain as

$$\begin{aligned} E(s) &= \frac{\tau(s)}{T_c}\frac{s}{s+K_d g_c F(s)} \\ &= \frac{A}{s}\frac{s}{s+K_d g_c \frac{\alpha}{s+\alpha}} \\ &= \frac{A(s+\alpha)}{s^2+\alpha s+\alpha K_d g_c} \\ &= \frac{A(s+\alpha)}{(s+a)^2+\omega_n^2} \end{aligned} \tag{7.36}$$

where we have substituted $a = \frac{\alpha}{2}$ and $\omega_n = \sqrt{aK_d g_c - a^2}$. Taking the inverse Laplace transform

$$e(t) = Ae^{-at}\left[\cos\omega_n t + \frac{a}{\omega_n}\sin\omega_n t\right] \tag{7.37}$$

Thus, larger values of α result in faster response times. Recalling the loop filter given above:

$$|(\omega)| = \frac{1}{\sqrt{1+\frac{\omega^2}{\alpha^2}}} \tag{7.38}$$

we can see that increasing α will improve the response time but ill correspond to a larger loop filter bandwidth which will degrade the noise performance.

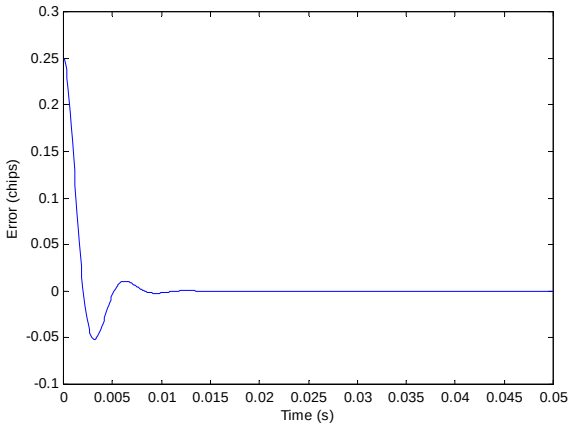


Figure 7.17: Example Error Signal with Reduced Bandwidth Filter

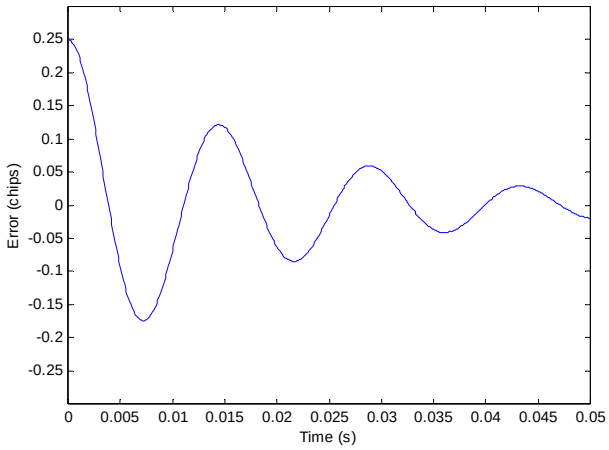


Figure 7.18:

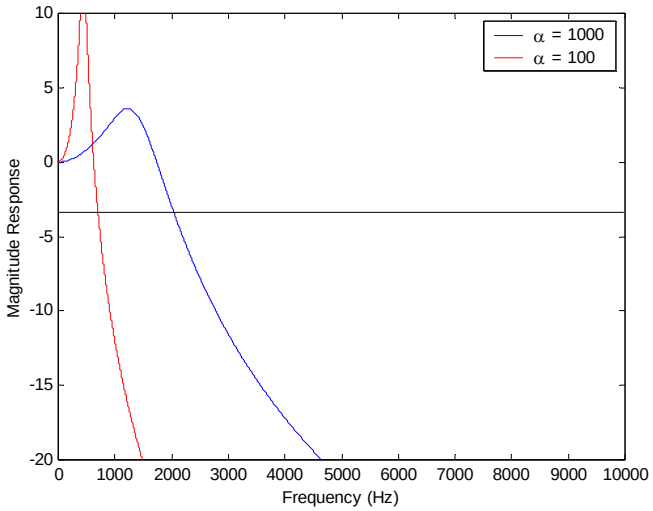


Figure 7.19: Comparison of Filter Magnitude Responses for Example

As an example, consider a low pass loop filter with a bandwidth of 1kHz. Again assume that the input is a step change of 0.25 T_c. The tracking error is plotted in Figure 7.17. We can see that the loop tracks very quickly. If the loop filter bandwidth is reduced to 100Hz, the loop will track more slowly as seen in Figure **??**. A comparison of the magnitude response of the two filters is given in Figure 7.19.

Finally, let us consider a design problem. Let us assume that we have a non-coherent DLL with a first order low pass loop filter. Let us set $\Delta = 1$ and assume that the IF bandwidth is $1MHz$. If the system requires a delay estimate to be within 1/16 of a chip in 1ms, what choice of α will minimize the tracking jitter?

To solve this, we first recall that the tracking jitter is related to the loop and IF SNR's by

$$\sigma_n^2 = \left(\frac{4}{\rho_{IF}} + 1\right)\frac{W_L}{2\rho_L B_n}$$

Thus, we want to minimize the loop bandwidth to minimize the jitter. However, the error signal is

$$e(t) = Ae^{-at}\left[\cos\omega_n t + \frac{a}{\omega_n}\sin\omega_n t\right] \tag{7.39}$$

Examining the envelope, we want

$$Ae^{-a*(0.001)} \leq \frac{1}{16} \tag{7.40}$$

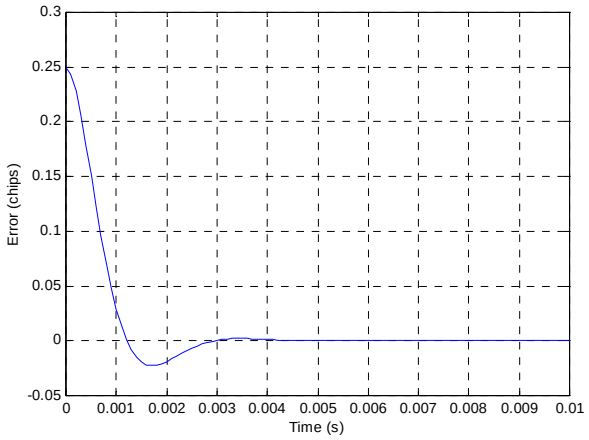


Figure 7.20: Example Error Response

Solving for α we find that we need $\alpha \geq 2750$. Thus, the smallest value of α that satisfies our requirement is 2750. Choosing $\alpha = 2800$ results in the response plotted in Figure 7.20. We can see that the error is less than 1/16 th of a chip by 1ms. The loop filter is plotted in Figure **??**. The Loop bandwidth is approximately 2800Hz. Thus, the tracking jitter can be found as $\left(\frac{4}{\rho_{IF}} + 1\right) \frac{2800}{2\rho_{IF}}$. The resulting plot of tracking jitter is plotted in Figure 7.22.

7.6 Tracking with Frequency Hopping

Tracking in frequency hopped systems is very much like direct sequence systems. A delay lock loop for frequency hopped systems is plotted in Figure 7.23. The loop removes the frequency hopping using delayed and advanced versions of the frequency hopping signal. The resulting energy of the two branches is filtered and a difference signal is formed which controls the timing of the hopping signal. To illustrate how the loop functions consider a frequency hopped signal with arbitrary modulation given in Figure **??**.

When the timing of the despreading signal is properly aligned, the resulting signal is dehopped into the original frequency band. A despread signal with improper timing will result in some of the signal energy outside of the original frequency band as shown in Figure 7.25 since the frequency of the dehopping signal will not coincide with the incoming signal for the entire chip time. In this example the estimated delay is smaller than the true delay. The early branch has a delay which is lower by some amount than the on time despreading branch. This results in even less energy as shown in Figure 7.26. However, the late branch will result in more despread energy since it is closer to the true delay

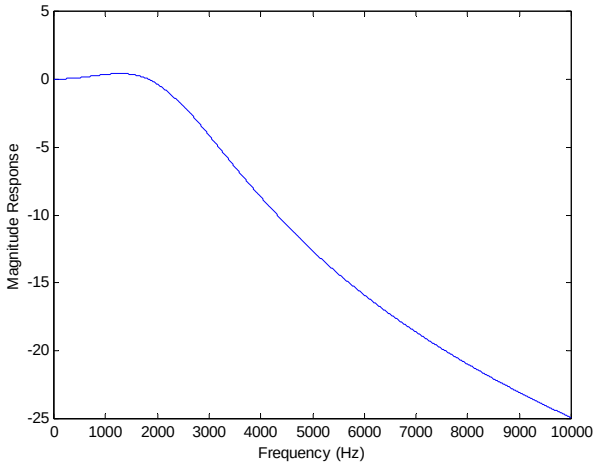


Figure 7.21:

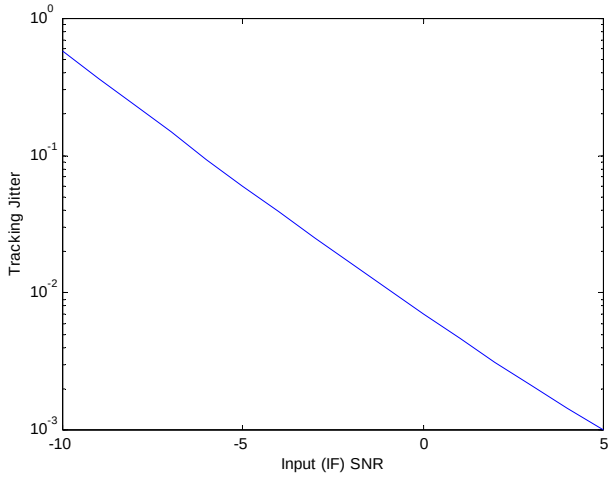


Figure 7.22:

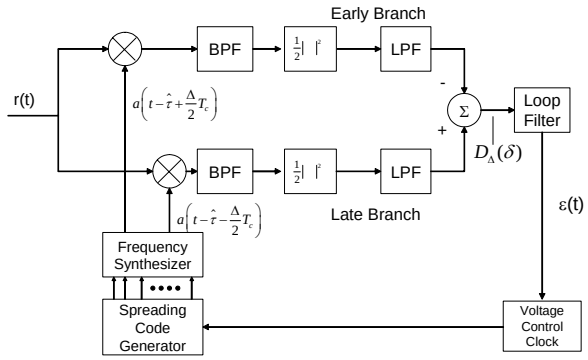


Figure 7.23: Delay Lock Loop for Frequency Hopped Systems

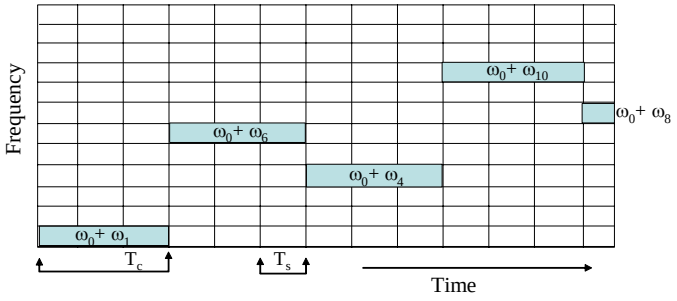


Figure 7.24: Example of the Received Signal Spectrum Occupancy for Frequency Hopped System

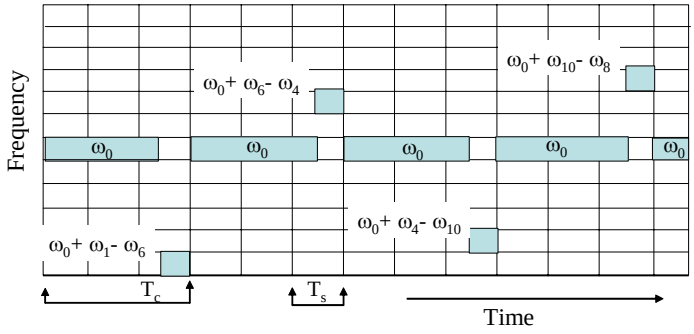


Figure 7.25: Example of the Received Signal Spectrum Occupancy for Frequency Hopped System with Improper Synchronization

as shown in Figure 7.27. By taking the difference between late branch and the early branch, the result is a positive number since the late energy is greater than the early energy. The delay estimate is thus increased, which is the proper change.

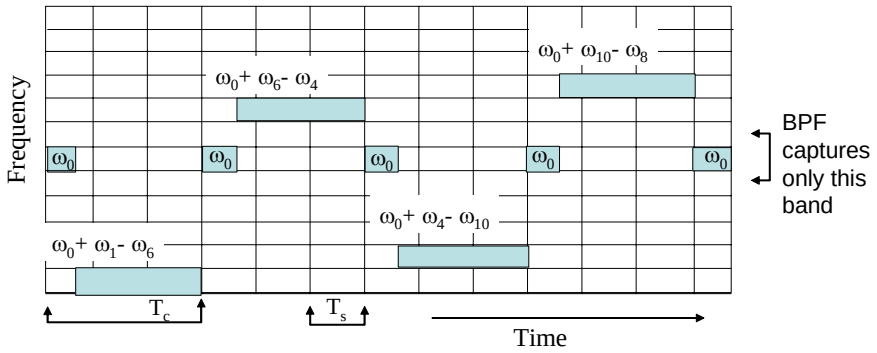


Figure 7.26: Example of the Received Signal Spectrum Occupancy for Early Branch of Frequency Hopped Tracking Loop

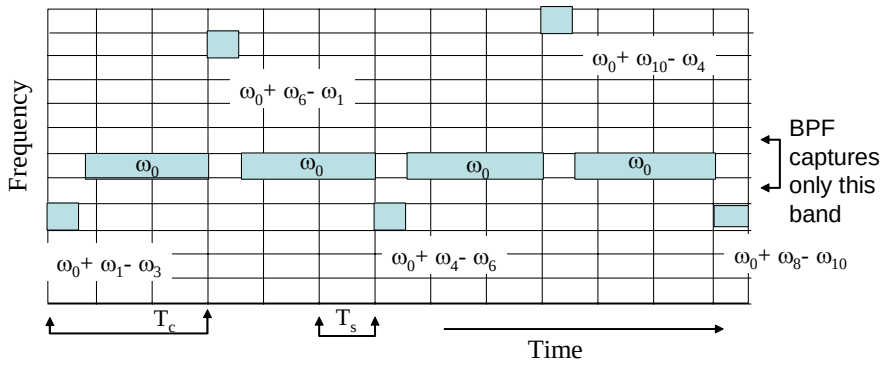


Figure 7.27: Example of the Received Signal Spectrum Occupancy for Early Branch of Frequency Hopped Tracking Loop

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