



COLLEGE OF ENGINEERING & TECHNOLOGY

Department : Electronics & Communications Engineering

Lecturer : Prof. Mohamed Essam Khedr

GTA : Eng. Hatem Abou-zeid

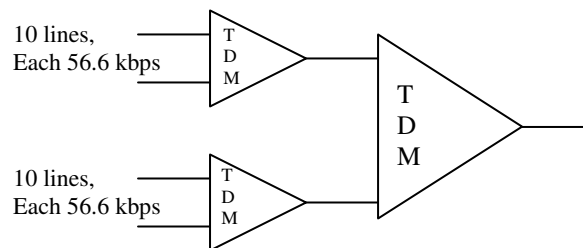
Course : Communication Networks

Course Code : EC 553,

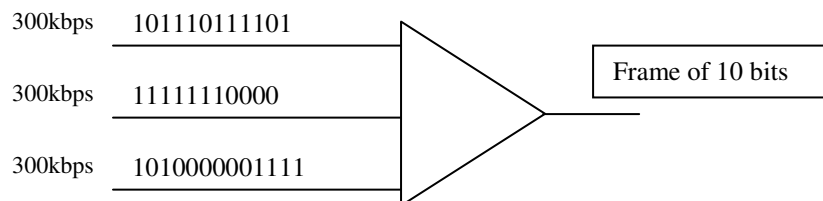
url: <http://www.aast.edu/~khedr/Courses/Undergraduate/Communication%20Networks%20EC553/>

Sheet (2)- Circuit & Packet Switching

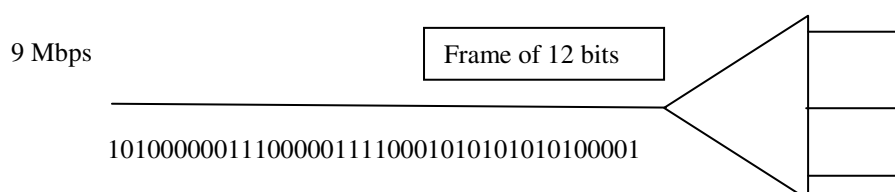
- 1- We have multiplexed 100 computers using synchronous TDM. If each computer sends data at the rate of 14.4 Kbps, what is the minimum bit rate of the line? Can a T-1 line handle this situation?
- 2- What is the minimum bit rate of each line in the below figure if we are using synchronous TDM? Ignore framing (synchronization) bits.



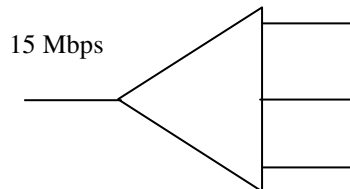
- 3- The figure below shows a multiplexer. If the slot is only 10 bits long (3 bits taken from each input plus 1 framing bit), what is the output bit stream? What is the output bit rate? What is the duration of each bit in the output line? How many slots are sent per second? What is the duration of each slot?



- 4- The figure below shows a demultiplexer. If the input slot is 12 bits long (ignore framing bits), what is the bit stream in each output? What is the bit rate for each output line?



- 5- The below figure shows an inverse multiplexer. If the input data rate is 15 Mbps, what is the rate for each line? Can we use the service of T-1 lines for this purpose? Ignore the framing bits.



- 6- Explain the flaw in the following reasoning: Packet switching requires control and address bits to be added to each packet. This introduces considerable overhead in packet switching. In circuit switching, a transparent circuit is established. No extra bits are needed. Therefore, there is no overhead in circuit switching. Because there is no overhead in circuit switching, line utilization must be more efficient than in packet switching.

- 7- Define the following parameters for a switching network:

N = number of hops between two given end systems

L = message length in bits

B = data rate, in bits per second, on all links

P = fixed packet size, in bits

H = overhead (header) bits per packet

S = call setup time (circuit switching or virtual circuit) in seconds

D = propagation delay per hop in seconds

- a. For $N=4$, $L=3200$, $B=9600$, $P=1024$, $H=16$, $S=0.2$, $D=0.001$, compute the end-to-end delay for circuit switching, virtual circuit packet switching, and datagram packet switching. Assume that there are no acknowledgments. Ignore processing delay at the nodes.
- b. Derive general expressions for the three techniques of part (a), taken two at a time (three expressions in all), showing the conditions under which the delays are equal.
- 8- What value of P , as a function of N , L , and H , results in minimum end-to-end delay in a datagram network? Assume that L is much larger than P , and D is zero.
- 9- Assuming no malfunction in any of the stations or nodes of a network, is it possible for a packet to be delivered to the wrong destination?